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10/029,101	12/20/2001	Richard L. Woodin	XDEV1140	8517

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EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/029,101

Applicant(s)

WOODIN ET AL.

Examiner

José R Díaz

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 18 September 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) 1-6 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 7-28 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

➤ Applicant's election without traverse of Group II (claims 7-28) in Paper No. 6 is acknowledged.

### ***Drawings***

➤ The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: the reference "40" in lines 2 of page 10. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Rejections - 35 USC § 102***

➤ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

➤ Claims 7-8 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Kiritani (US 2002/0052102 A1).

Regarding claim 7, Kiritani teaches a process for forming an electrical connection comprising the steps of: forming a first metal-containing layer (63) over a silicon carbide

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(61) (see Fig. 9), and annealing the first metal-containing layer (63) and the silicon carbide (61) (see paragraph [0091]).

Regarding claim 8, Kiritani teaches that the first metal-containing layer comprises aluminum (see paragraph [0091]).

Regarding claim 15, Kiritani teaches that the silicon carbide (61) is p-type doped (see Fig. 9).

### ***Claim Rejections - 35 USC § 103***

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➤ Claims 9-14, and 16-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiritani (US 2002/0052102 A1) in view of Hall et al. (US Patent No. 3,900,598).

Regarding claims 9, 12, 13, 16-17, 19, 22-23, and 26-28, Kiritani teaches a process for forming an electrical connection comprising the steps of: forming a first metal-containing layer (63) over a silicon carbide (61) (see Fig. 9), and annealing the first metal-containing layer (63) and the silicon carbide (61) (see paragraph [0091]). Furthermore, Kiritani teaches that the annealing process is performed at a temperature higher than 300 °C (see paragraph [0091]). However, Kiritani fails to teach the step of performing an annealing process at temperature of about 300-660 °C for a time period of at least 10 hours. Hall et al. teach a well-known method of forming ohmic contact comprising an annealing step performed at a temperature of 500 °C in a vacuum (see col. 2, lines 37-60 and col. 4, lines 32-47). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kiritani to include the step of annealing at a temperature of about 500 °C to form an ohmic contact. The ordinary artisan would have been motivated to modify Kiritani in the manner described above for at least the purpose of providing an ohmic contact having reduced silicon solubility and improved etching properties. With regards to the time period of the annealing step, Hall et al. provide a general teaching of performing such an annealing process (see col. 2, lines 48-60 and col. 4, lines 32-47). Therefore, it would have been obvious to one of ordinary skill in the art to vary the time period of the annealing process, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. The ordinary artisan would have been

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- motivated to modify Kiritani in the manner described above for at least the purpose of providing a semiconductor device with an improved ohmic contact.

Regarding claims 10 and 20, Kiritani is silent with respect to the properties of the aluminum material used as the first metal-containing layer (see paragraph [0091]). Hall et al. teach that is well known in the art to use pure aluminum as the first metal-containing layer (18) (see col. 2, lines 32-35). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kiritani to include a first metal-containing layer formed of a pure aluminum material. The ordinary artisan would have been motivated to modify Kiritani in the manner described above for at least the purpose of providing a semiconductor device with an improved ohmic contact.

Regarding claims 14 and 24, Kiritani does not teach alloying the aluminum layer. Hall et al. teach that is well known in the art to performed the annealing step to form aluminum-substrate alloy (see col. 2, lines 42-44 and 50-60; and col. 4, lines 32-47). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kiritani to include the step of annealing the semiconductor device to form an aluminum-substrate alloy. The ordinary artisan would have been motivated to modify Kiritani in the manner described above for at least the purpose of providing a semiconductor device with an improved ohmic contact.

Regarding claim 18, Kiritani does not teaches the step of etching and patterning the metal containing layer. Hall et al. teach that is well known in the art to etch and

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- pattern the metal containing layer (see col. 2, lines 40-47; col. 3, lines 48-55; and col. 4, lines 32-47).

Regarding claims 11 and 21, Kiritani is silent with respect to the properties of the aluminum material used as the first metal-containing layer (see paragraph [0091]). Hall et al. teach that is well known in the art to add a relative small percentage (e.g. less than 10%) of another metal to the aluminum material to form the first metal-containing layer (18) (see col. 3, lines 46-59). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kiritani to include a first metal-containing layer formed of a aluminum material having a relative small percentage of another metal. The ordinary artisan would have been motivated to modify Kiritani in the manner described above for at least the purpose of providing a semiconductor device with an improved ohmic contact.

Regarding claim 25, Kiritani teaches that the silicon carbide (61) is p-type doped (see Fig. 9).

### ***Correspondence***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for

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- the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD  
November 30, 2002



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
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